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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/695,311	10/25/2000	Minoru Oohira	198778US2DIV	2441
22850	7590 11/19/2003		EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET			ZARNEKE, DAVID A	
ALEXANDRIA, VA 22314			ART UNIT	PAPER NUMBER
			2027	

DATE MAILED: 11/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)				
055 4 4	_	09/695,311	OOHIRA ET AL.				
Office Action	Summary	Examiner	Art Unit				
		David A. Zarneke	2827				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address P riod for Reply							
THE MAILING DATE OF 1 - Extensions of time may be available after SIX (6) MONTHS from the m - If the period for reply specified abo - If NO period for reply is specified a - Failure to reply within the set or ex-	FHIS COMMUNICATION. le under the provisions of 37 CFR 1.1 ailing date of this communication, we is less than thirty (30) days, a reply bove, the maximum statutory period v lended period for reply will, by statute ere than three months after the mailing.	Y IS SET TO EXPIRE 3 MONTH(38(a). In no event, however, may a reply be tin y within the statutory minimum of thirty (30) day, within the statutory minimum of thirty (30) day with apply and with surper SIX (8) MONTHS from cause the application to become ABANDONE date of this communication, even if timely filed	nely filed s will be considered time the mailing date of this of	ly. communication.			
1) Responsive to com	munication(s) filed on	<u>_</u> .					
2a) This action is FINA	L . 2b)⊠ Th	is action is non-final.					
Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213. Disposition of Claims							
4)⊠ Claim(s) <u>8-14</u> is/are	nending in the application						
	im(s) is/are withdraw						
		m nom consideration.					
5)							
7) Claim(s) is/are rejected.							
8) Claim(s) are		r election requirement					
Application Papers		r diddion roquirement.					
9)☐ The specification is objected to by the Examiner.							
10) ☐ The drawing(s) filed on is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.							
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
11) ☐ The proposed drawing correction filed on is: a) ☐ approved b) ☐ disapproved by the Examiner.							
If approved, corrected drawings are required in reply to this Office action.							
12) The oath or declaration is objected to by the Examiner.							
Priority under 35 U.S.C. §§ 1							
13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).							
a) ☐ All b) ☐ Some * c) ☐ None of:							
 Certified copie 	es of the priority document	s have been received.					
2. Certified copies of the priority documents have been received in Application No							
 Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). See the attached detailed Office action for a list of the certified copies not received. 							
14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).							
a) The translation of the foreign language provisional application has been received. 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.							
Attachment(s)	s. a olalii ioi dolllest						
1) Notice of References Cited (PTO-892) 1) Notice of Draftsperson's Patent Drawing Review (PTO-948) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statements (NPTO-1449) Pager No(s)							

Art Unit: 2827

DETAILED ACTION

Response to Arguments

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Therefore, the rejection of claims 8-10 has been withdrawn.

Further, upon further consideration, the previously noted allowability of claims 11-14 has been removed.

New rejections of pending claims 8-14 are discussed below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this tille, if the differences between the subject matter sought to be patented and the prior at are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

- Determining the scope and contents of the prior art.
- 2. Ascertaining the differences between the prior art and the claims at issue.
- 3. Resolving the level of ordinary skill in the pertinent art.
- Considering objective evidence present in the application indicating obviousness or nonobviousness.

Art Unit: 2827

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Steffen, US Patent 5,041,395.

Steffen teaches a method for producing discrete semiconductor devices, comprising the steps of:

forming a plurality (3, 45+) of sets of die bond pads (12) and wire bond pads (14) by fastening an electrically conductive metal sheet at specified positions on the back of an insulating sheet and making apertures in the insulating sheet on the metal sheet (figure 3),

packaging the discrete semiconductor elements, said packaging step comprising fastening the back of the discrete semiconductor elements (26) on the die bond pads and electrically connecting the electrodes of the discrete semiconductor elements and the wire bond pads (figure 4),

Art Unit: 2827

sealing the plurality of discrete semiconductor elements installed on the insulating sheet with an integral sealing resin by sealing the packaging surface of the insulating sheet with the resin (figure 5), and

dividing the sealing resin into the discrete semiconductor devices by cutting off the sealing resin around the discrete semiconductor elements (3, 50+).

Steffen, which teaches a metal grid with punched zones (3, 62+), fails to teach the use of multiple electrically conductive metal sheets to form the bond pads and die pads.

Barring a showing of unexpected results, it would have been obvious to one of ordinary skill in the art that punching, or even etching, of a metal grid to form die pads and wire bond pads is an equivalent technique to supplying multiple sheets, one for the die pad and others for the wire bond pads.

The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution. Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

Regarding claim 9, Steffen teaches fastening a back side electrode of the discrete semiconductor device onto the corresponding die bond pad to electrically connect the die bond pad and the back side electrode (figure 4).

With respect to claim 10, Steffen teaches cutting off the sealing resin around a plurality of discrete semiconductor elements grouped as a single body such that at least

Art Unit: 2827

one of the discrete semiconductor devices comprises a plurality of the discrete semiconductor elements sealed with the integral resin (3, 50+).

Claims 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fjelstad, US Patent 6,001,671.

Fjelstad teaches a method for producing a discrete semiconductor device (figures 7A to 7G-2), comprising the steps of:

packaging a plurality of discrete semiconductor elements (420), said packaging step comprising fastening the back of the discrete semiconductor elements onto an electrically conductive metal sheet (400) and connecting electrically an electrode of each discrete semiconductor element to a specified position of the metal sheet (410), sealing the packaging surface of the metal sheet with an integral sealing resin

sealing the packaging surface of the metal sheet with an integral sealing resin (440),

cutting off the metal sheet by cutting therein from the back to turn the metal sheet into die bond pads and wire bond pads which are arranged at intervals (figure 7G-1 &/or 7G-2), and

dividing the discrete semiconductor devices by cutting off the sealing resin around the discrete semiconductor elements.

While Figures 7A to 7G-2 of Fjelstad do not specifically teaching the use of a plurality of semiconductor elements and dividing them into separate packages, figures 1A to 1G-1 and 5A-5H teach the use of multiple devices divided into individual packages.

Art Unit: 2827

Regarding claim 12, Fjelstad teaches fastening the back electrode of the discrete semiconductor elements onto the metal sheet and electrically connecting the metal sheet and the back electrode (figure 7D).

With respect to claim 13, Fjelstad teaches cutting off the sealing resin around a plurality of discrete semiconductor elements grouped as a single body, to divide the discrete semiconductor devices each carrying the plurality of discrete semiconductor elements being sealed with the integral resin (figures 1A to 1G-1 and 5A-5H).

As to claim 14, Fjelstad teaches cutting off the metal sheet comprises cutting off the metal sheet such that the die bond pads and/or the wire bond pads connected to the plurality of discrete semiconductor elements become an integral body, and the dividing step comprises cutting off the sealing resin around the discrete semiconductor elements which are formed so that the die bond pads and/or the wire bond pads connected to the plurality of discrete semiconductor elements become an integral body, thereby to obtain the discrete semiconductor device wherein the plurality of discrete semiconductor elements which share the die bond pads and/or the wire bond pads in common are sealed with the integral resin (see figures).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David A. Zarneke whose telephone number is (703)-305-3926. The examiner can normally be reached on M-F 10AM-6PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (703)-308-1233. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-308-6789.

David A. Zarneké

Primary Examiner AU2827

November 2, 2003